Remarks/Arguments

Applicant has received and carefully reviewed the Office Action mailed October 22. 2003. Claims 1, 3-10, and 12-27 remain pending. Claims 2 and 11 have been previously canceled, without prejudice. Reexamination and reconsideration are respectfully requested.

The undersigned would like to thank the Examiner for the courtesies extended during the telephone interview of March 14, 2005. Each of the independent claims was discussed. With respect to claim 1, the Examiner indicated that when Col is read very broadly, the flags register of Figure 5B may correspond to the digital value/at least one status bit of claim 1, and the condition evaluation block 572 of Figure 5B of Col may determine if the condition of the conditional jump instruction is satisfied without having to submit the condition of the conditional jump instruction to an arithmetic logic stage of the pipelines instruction processor. The Examiner recognizes that the flags register 561 and the conditional evaluation block 572 of Col both are activated after the conditional jump instruction is processed by the ALU 562.

To overcome this broad reading of claim 1, the Examiner suggested amending claim 1 to recite that the condition of the condition jump instruction is resolved before the conditional jump instruction reaches the ALU stage. The Examiner believed that such an amendment would likely overcome the rejection based on Col, but that another search may need to be done.

In view of the Examiner's comments, and to move the case along, claim 1 has been amended to recite:

in response to a conditional jump instruction, reading from the memory the digital value and the at least one status bit to ~~determine if~~ resolve whether the condition of the conditional jump instruction is satisfied before the conditional jump instruction reaches ~~without having to submit the condition of the conditional jump instruction to~~ an arithmetic logic stage of the pipelines instruction processor

Claim 10 has been similarly amended. In view of the foregoing, independent claims 1 and 10 are believed to be clearly patentable over the cited prior art. For similar and other reasons, dependent claims 3-9 and 12-18 are also believed to be clearly patentable over the cited prior art.

Turning now to claim 19. During the telephone interview, the undersigned pointed out a number of differences between claim 19 and the cited prior art. Claim 19 recites:

19. (Previously Presented) In a pipelined instruction processor that executes instructions including conditional jump instructions, one or more of the conditional jump instructions reading a digital value from memory to determine if the condition of the conditional jump instruction is satisfied, the improvement comprising:

a plurality of addressable registers, each of the addressable registers storing a value that includes a digital value and at least one jump status bit;

logic to access a current instruction, wherein the current instruction includes an address and a corresponding jump field, the address identifies one of the addressable registers and the corresponding jump field identifies a jump status bit of the at least one jump status bits within the identified addressable register;

a jump look-ahead controller for generating a jump look-ahead signal using the address that identifies one of the addressable registers and the jump field that identifies a jump status bit within the identified addressable register, the jump look-ahead signal is a function of the identified jump status bit;

tracking logic for tracking the addresses of a predetermined number of previous instructions in the pipelined instruction processor and comparing the addresses of each previous instruction to the address of the current instruction to generate a series of jump disable signals; and

conflict detection logic for generating a jump early signal using the jump look-ahead signal and the series of jump disable signals, the jump early signal initiates the conditional jump depending on the values of the jump disable signals.

In paragraph 21 of the Final Office Action, the Examiner rejected claims 19-22 and 24-27 under 35 U.S.C. 103(a) as being unpatentable over Watson et al. in view of Col. The Examiner states that Col suggests what Watson et al. is missing, including a current instruction that includes an address and a corresponding jump field, wherein the address identifies one of the addressable registers and the corresponding jump field identifies a jump status bit of the at least one jump status bits within the identified addressable register.

The Examiner provides a number of cites to Col. However, after carefully reviewing each of the cited portions of the Col, Applicants fail to see where an instruction is shown that includes an address and a corresponding jump field, wherein the address identifies one of the addressable registers and the corresponding jump field identifies a jump status bit of the at least one jump status bits within the identified addressable register. This was pointed out during the telephone interview.

In addition, and as noted above, claim 19 recites "a jump look-ahead controller" for generating a jump look-ahead signal using the address that identifies one of the addressable registers and the jump field that identifies a jump status bit within the identified addressable register, the jump look-ahead signal is a function of the identified jump status bit. As noted above, the Examiner appears to be equating the flags register 561 of Figure 5B of Col with the addressable registers recited in claim 19.

However, even under this interpretation, there does not appear to be any teaching or suggestion, in either Col or Watson, for using the flags register 561 to generate a jump look-ahead signal using the address that identifies one of the addressable registers and the jump field that identifies a jump status bit within the identified addressable register, the jump look-ahead signal is a function of the identified jump status bit, as recited in claim 19. In Col, a Branch Predictor 522 (see Figure 5A) is provided in the "translate" stage of the pipeline processor. However, there is no indication that the Branch Predictor 522 uses the contents of the flags register 561 to generate a jump look-ahead signal that is a function of the jump status bit, as recited in claim 19. Further, Watson does not appear to supply what Col is missing. Therefore, the combination of Watson and Col cannot render claim 19 obvious. In view of the foregoing, claim 19 is believed to be clearly patentable over Watson in view of Col. For similar and other reasons, dependent claims 20-26 are also believed to be clearly patentable over Watson in view of Col. For similar and other reasons, independent claim 27 is also believed to be clearly patentable over Watson in view of Col.

In view of the foregoing, it is believed that all pending claims 1, 2-10 and 12-27 are now in condition for allowance. Issuance of a notice of allowance in due course is respectfully requested. If a telephone conference would be of assistance, please contact the undersigned attorney at 612-359-9348.

Respectfully submitted,

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